

FIG. 1A

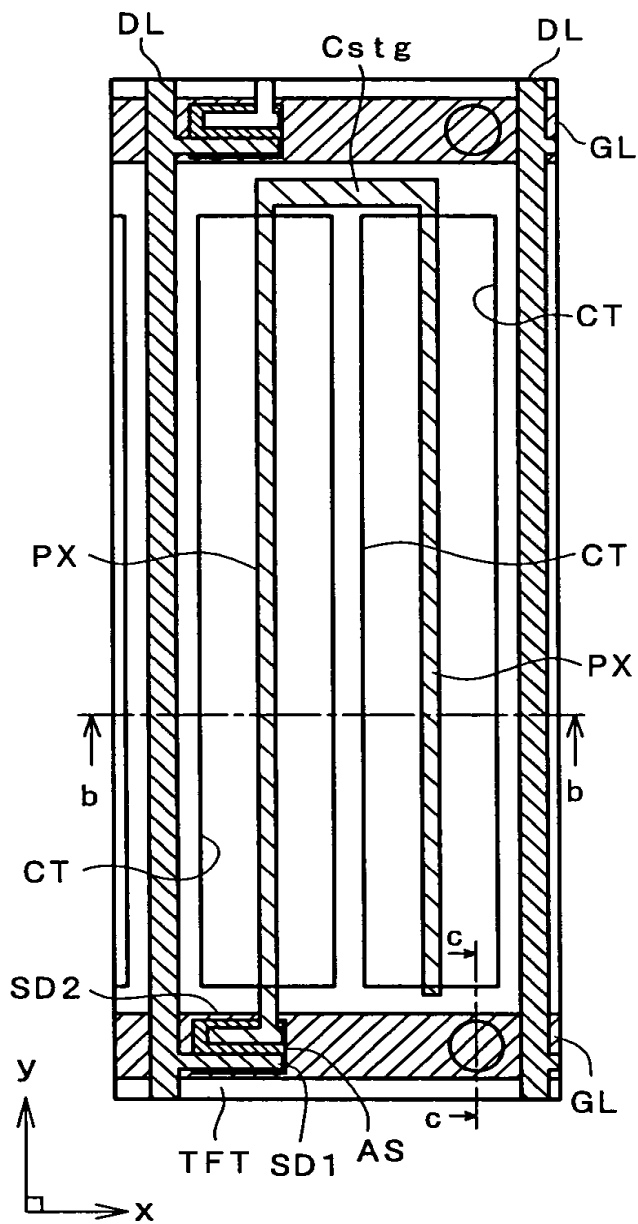


FIG. 1B

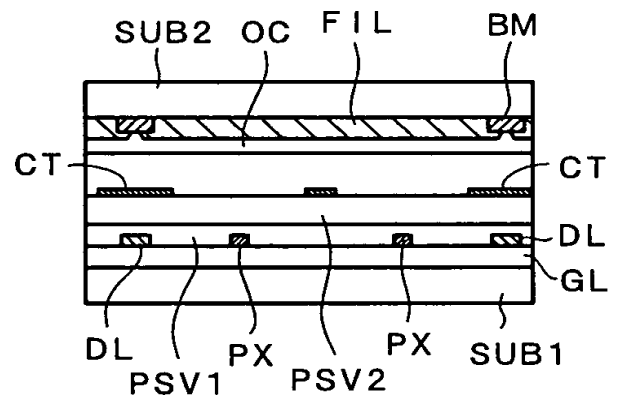


FIG. 1C

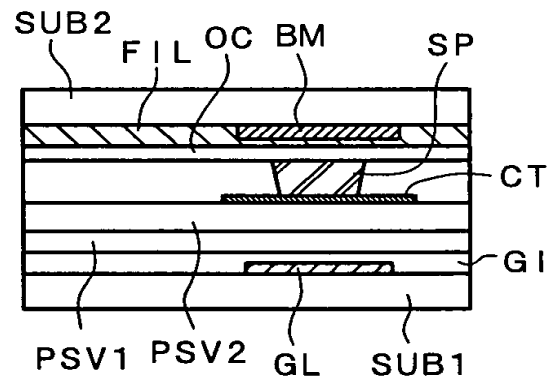
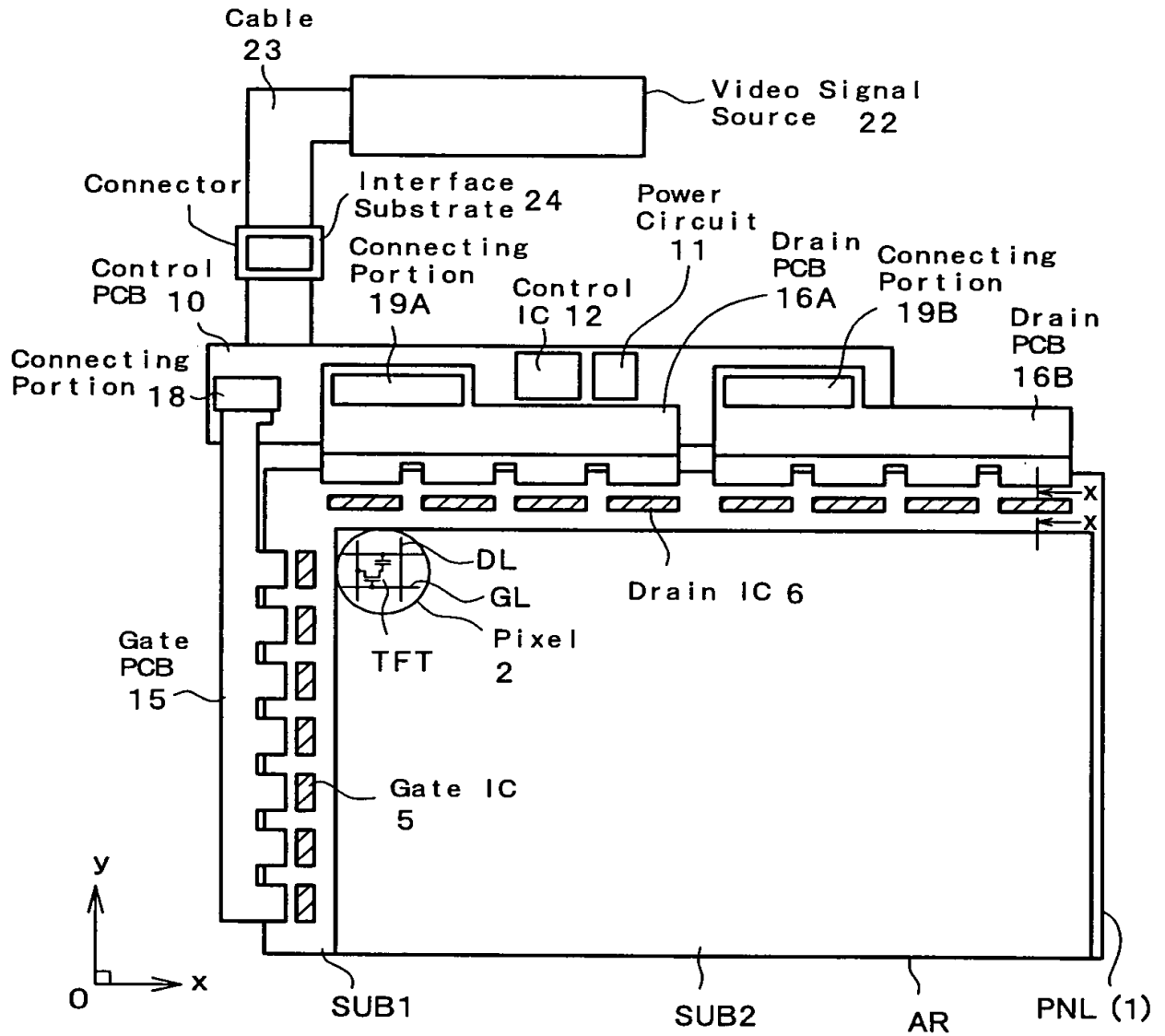


FIG. 2



A cross-sectional view of a semiconductor device. The device consists of a substrate (SUB1) at the bottom, which is divided into a central region and two side regions. The central region contains a series of layers: a gate layer (GL) with a central opening, a first polysilicon layer (PSV1), a second polysilicon layer (PSV2), a contact layer (CT), and a barrier metal layer (BM). The side regions are labeled SUB2. The device is characterized by several dimensions: $d1$ is the thickness of the PSV1 layer; $d2$ is the width of the central opening in the GL layer; $d3$ is the thickness of the CT layer; $d4$ is the width of the central opening in the BM layer. The layers are labeled with lines pointing to them: SUB1, SUB2, GL, PSV1, PSV2, CT, BM, and SP (which points to the central opening in the BM layer).

FIG. 4A

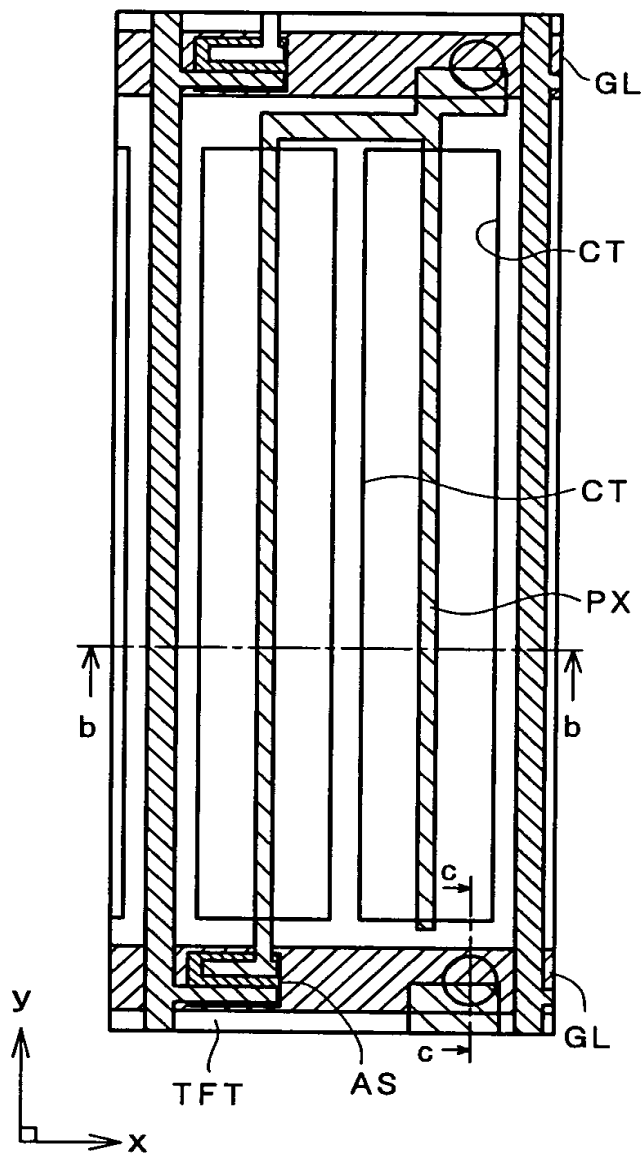


FIG. 4B

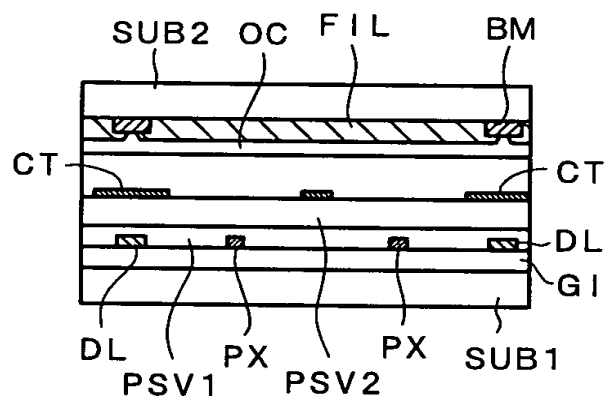


FIG. 4C

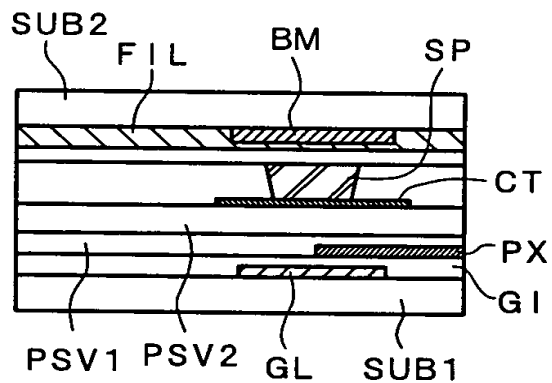


FIG. 5A

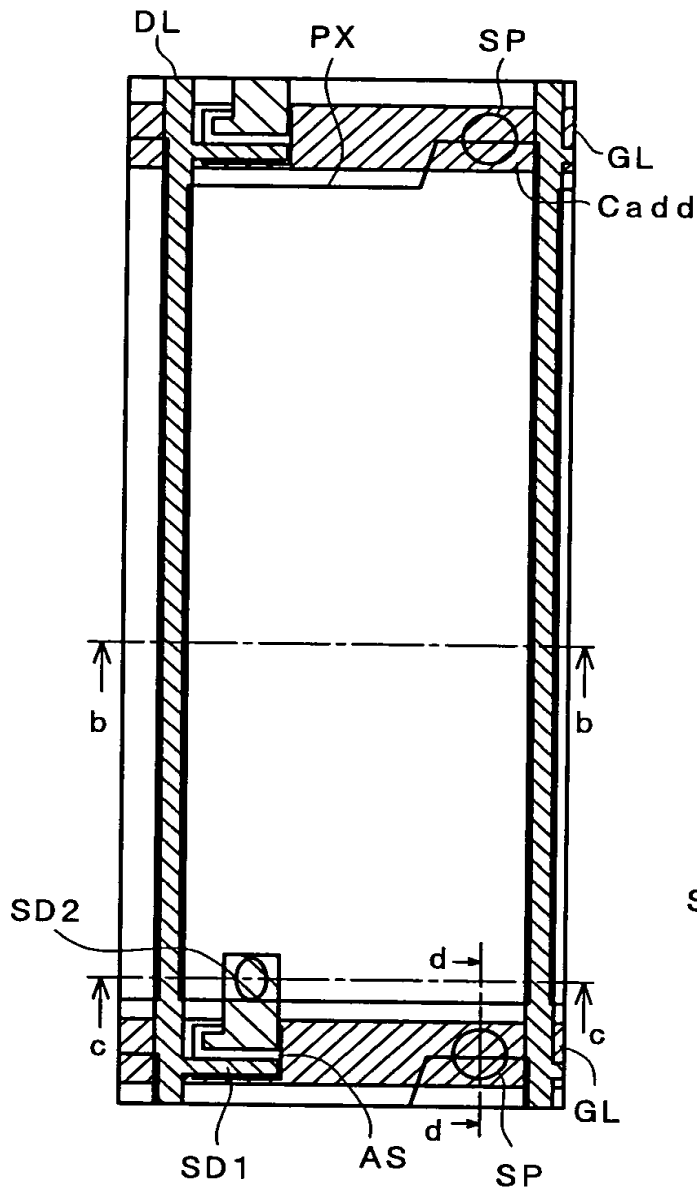


FIG. 5B

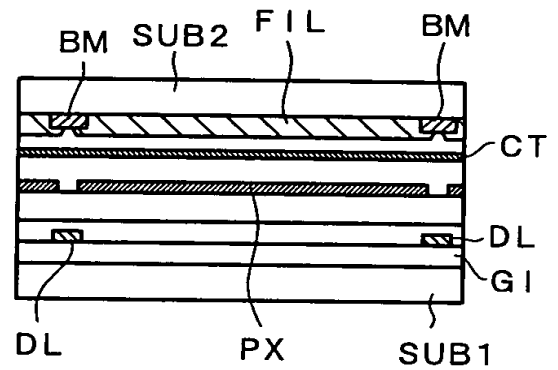


FIG. 5C

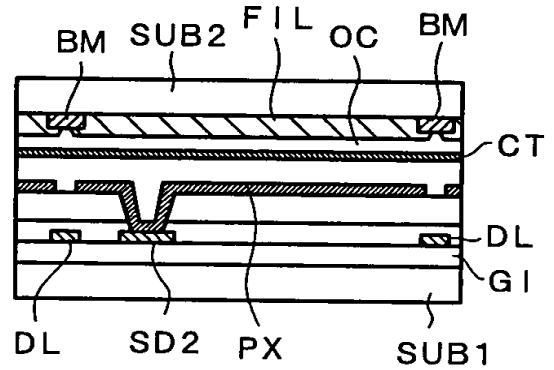


FIG. 5D

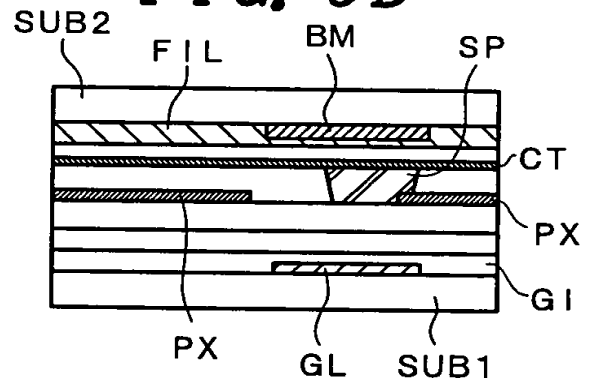


FIG. 6

Light leak area
around spacer: large

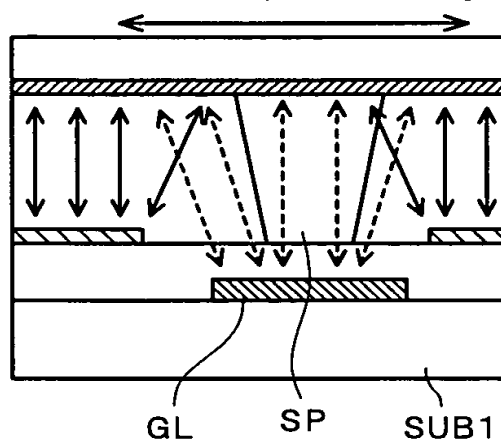


FIG. 7

Light leak area
around spacer: small

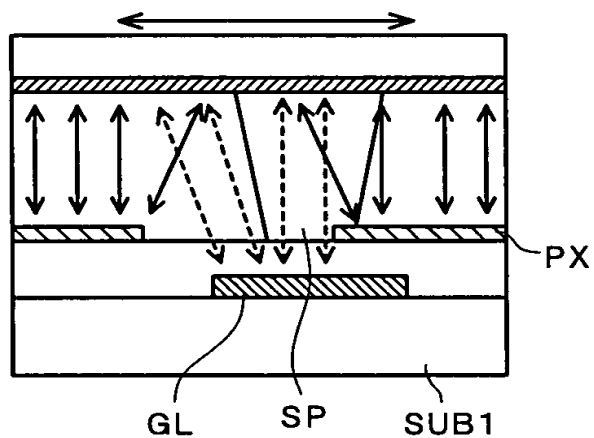


FIG. 8

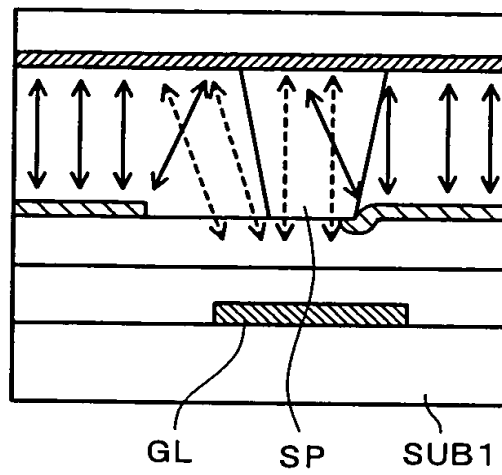


FIG. 9

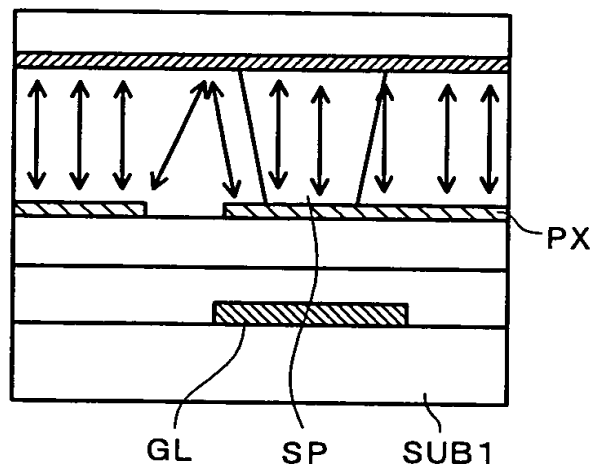


FIG. 10

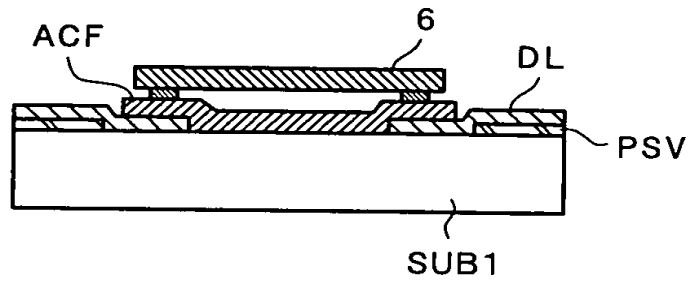


FIG. 11A

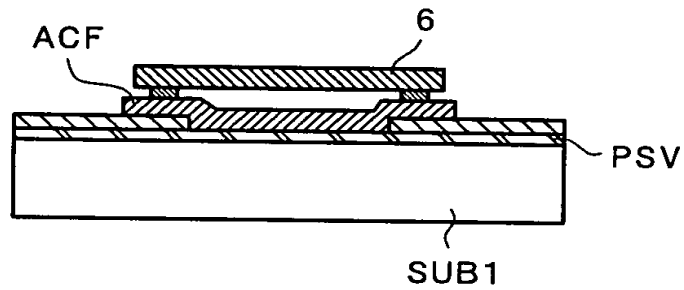


FIG. 11B

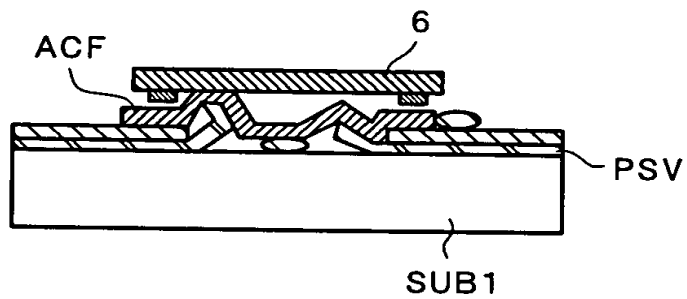


FIG. 12

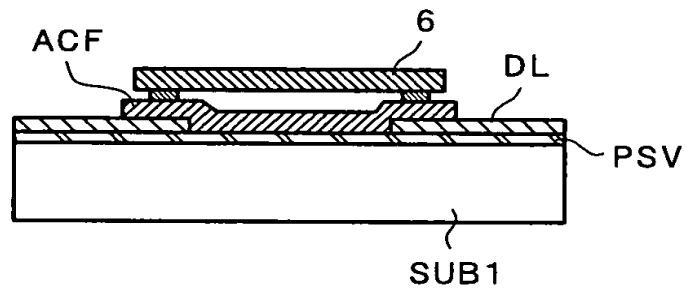


FIG. 13

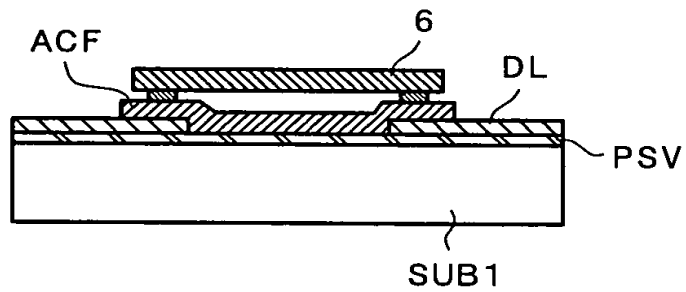


FIG. 14

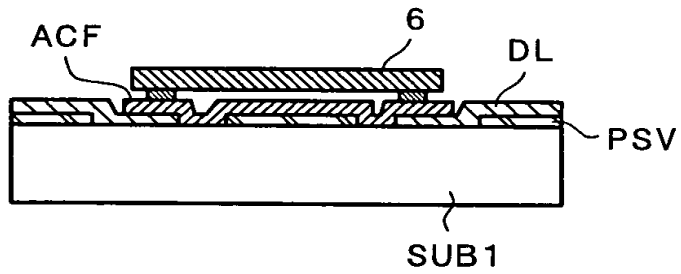


FIG. 15

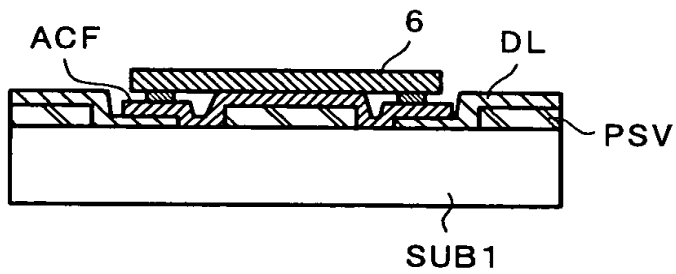


FIG. 16

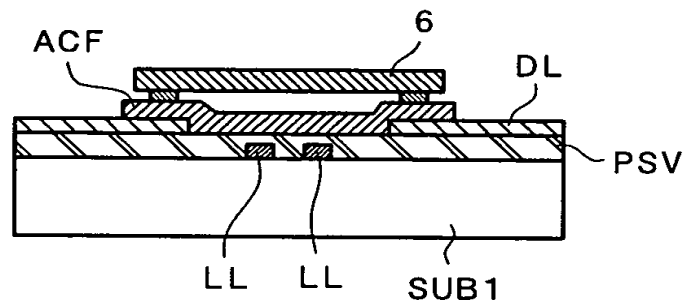


FIG. 17

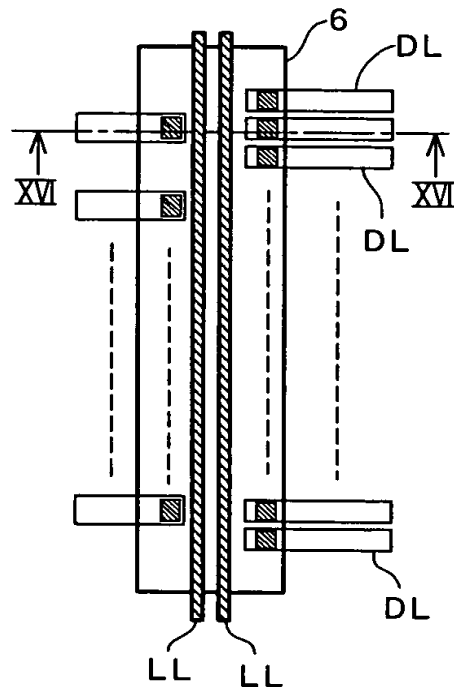


FIG. 18

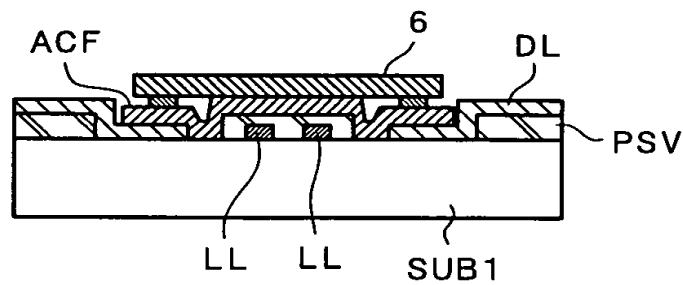


FIG. 19A

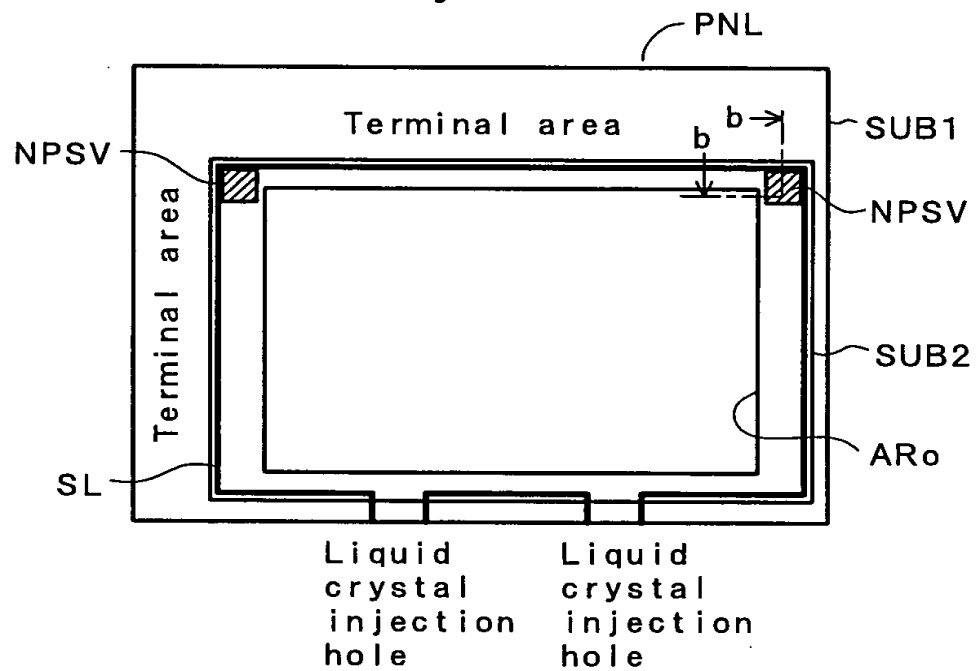


FIG. 19B

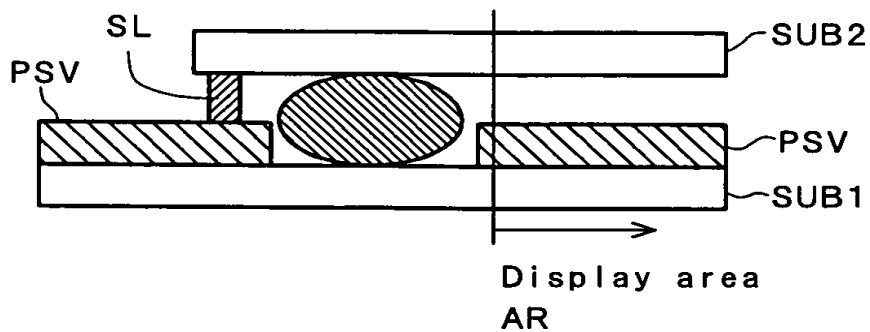


FIG. 20A

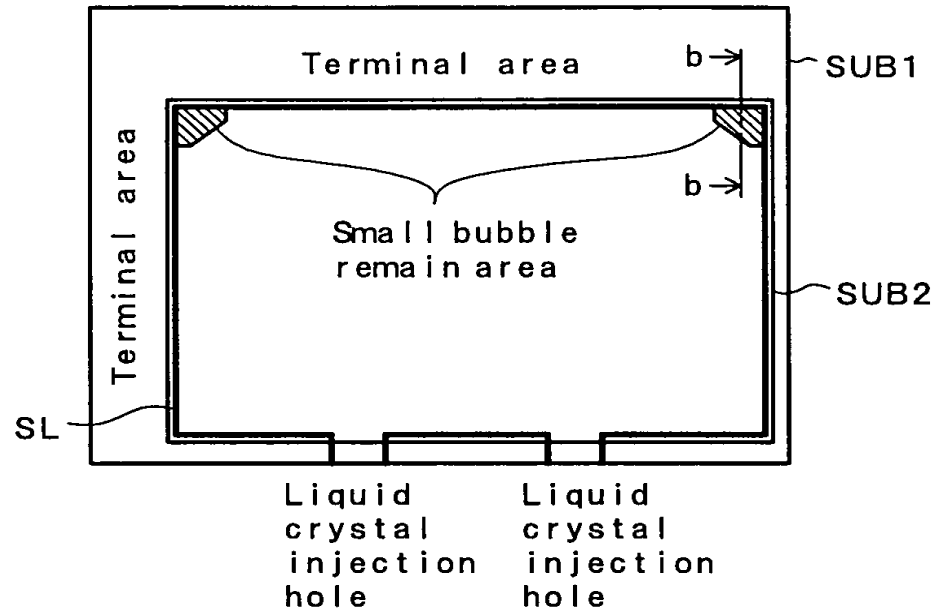


FIG. 20B

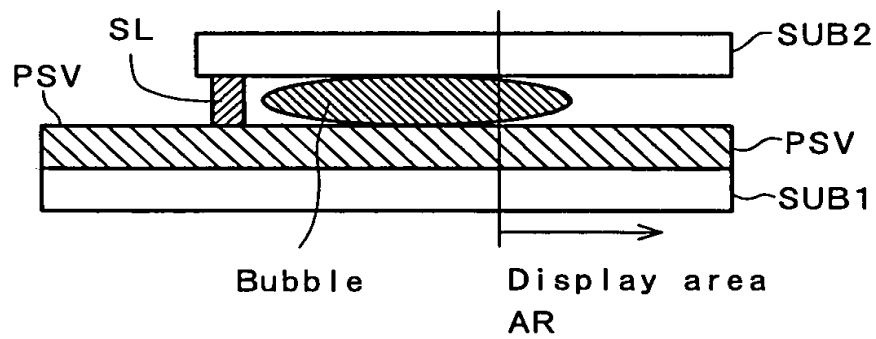


FIG. 21

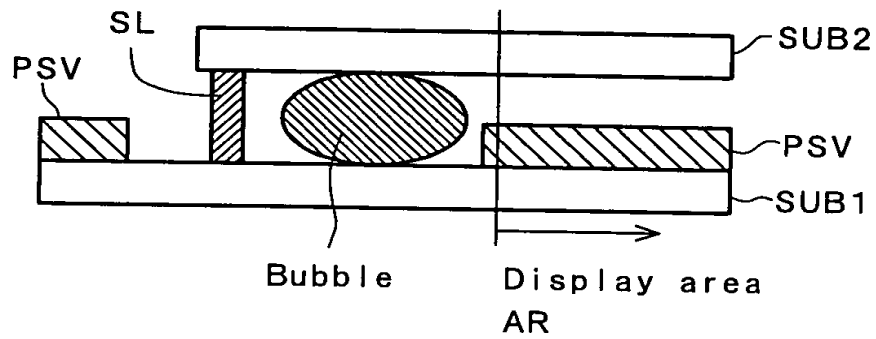


FIG. 22A

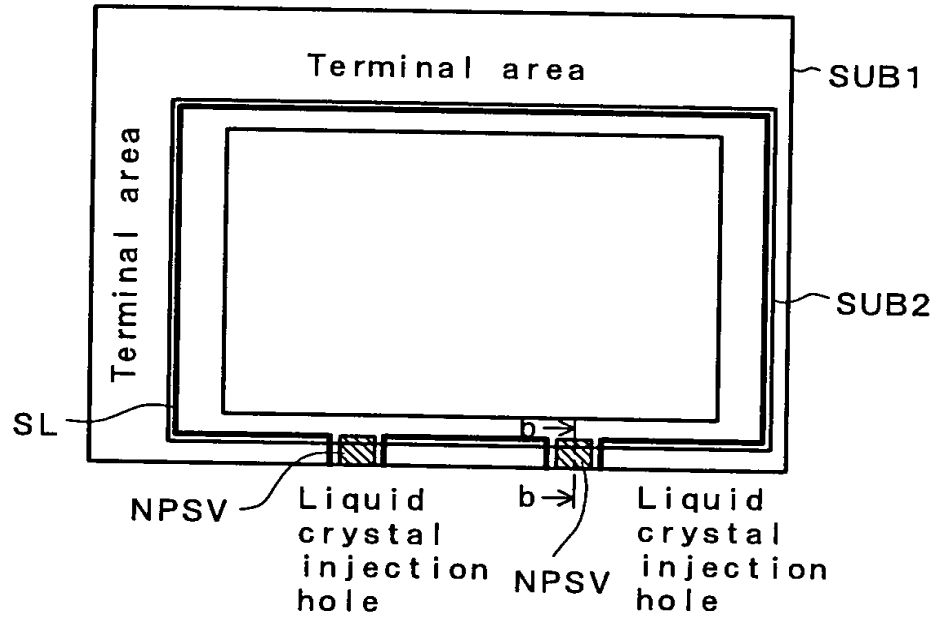


FIG. 22B

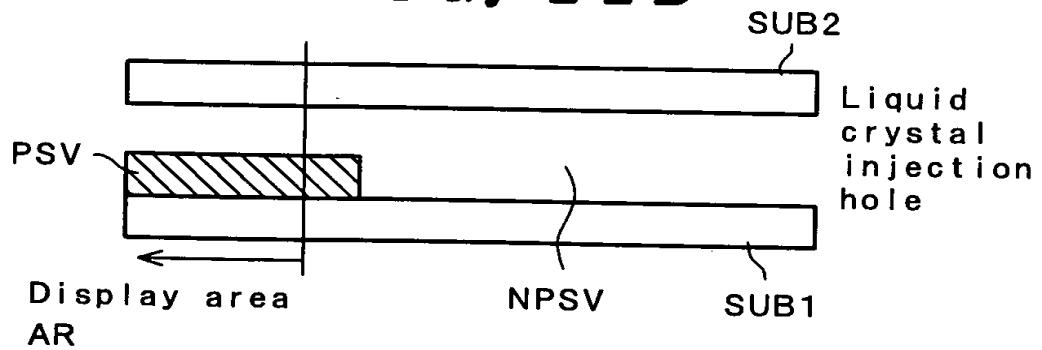


FIG. 23

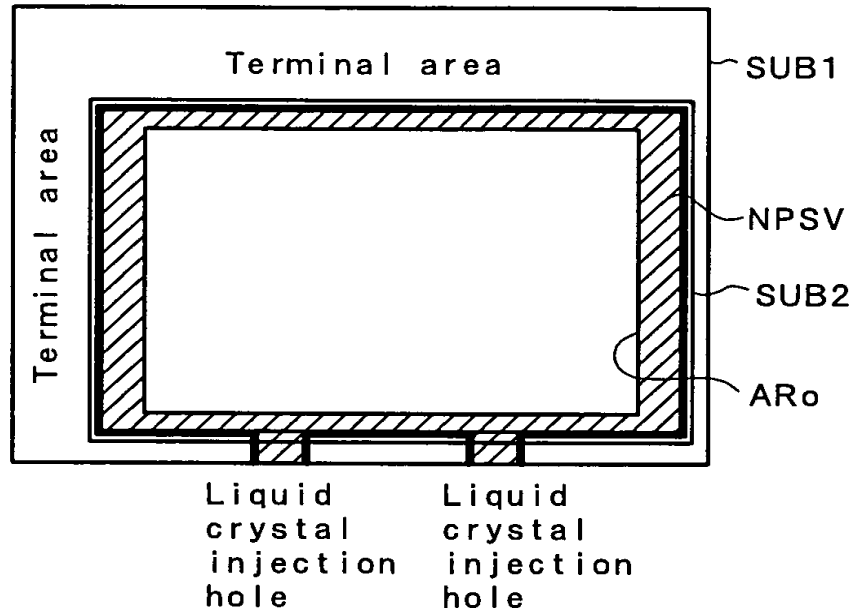


FIG. 24

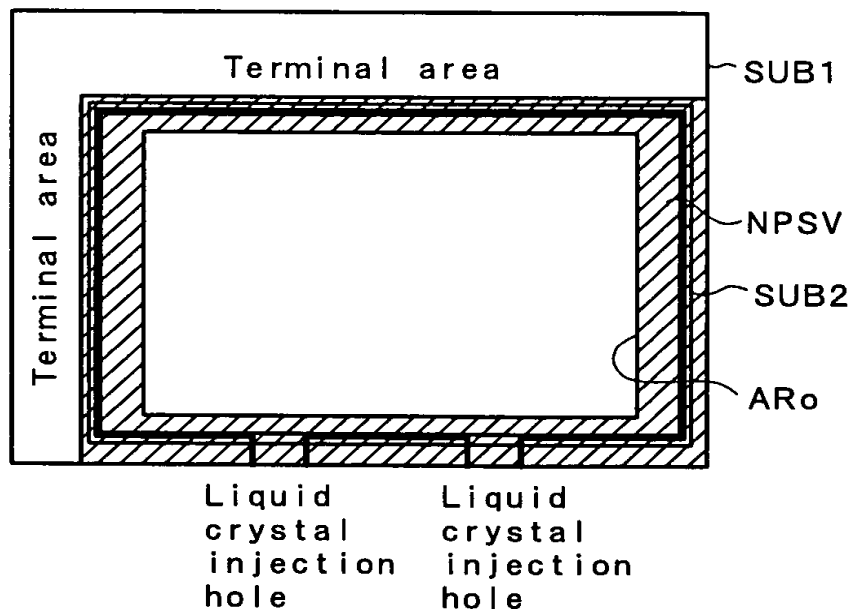


FIG. 25

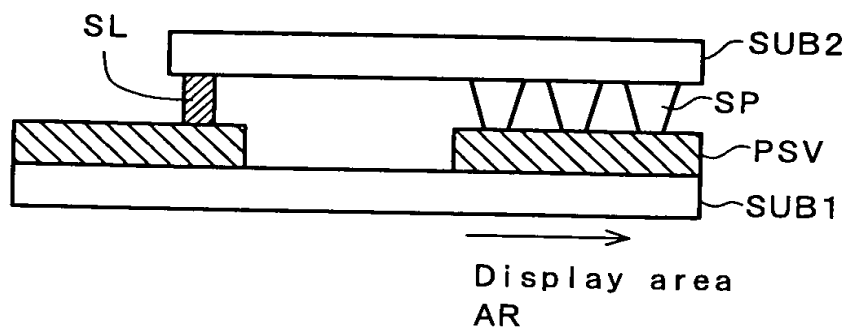


FIG. 26

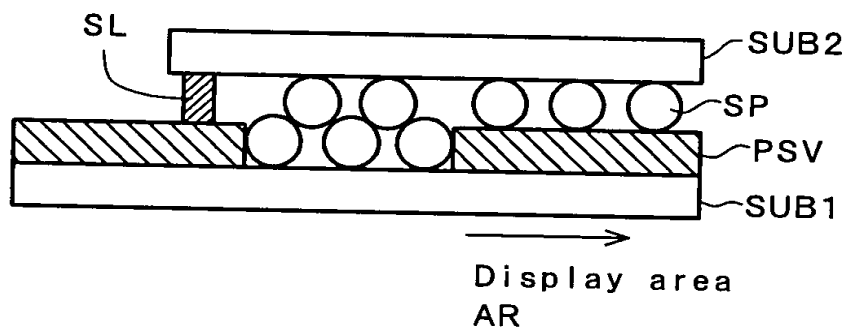


FIG. 27

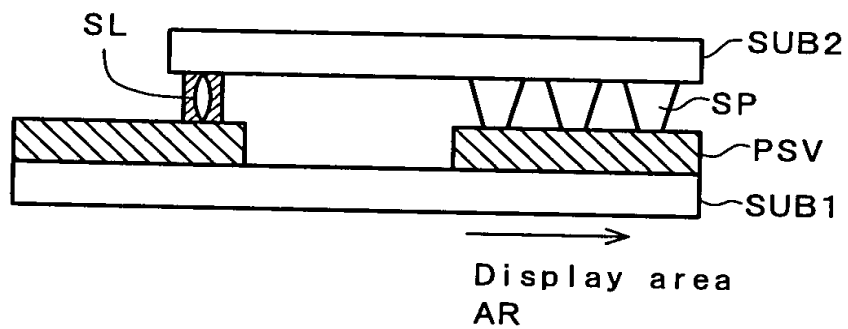


FIG. 28

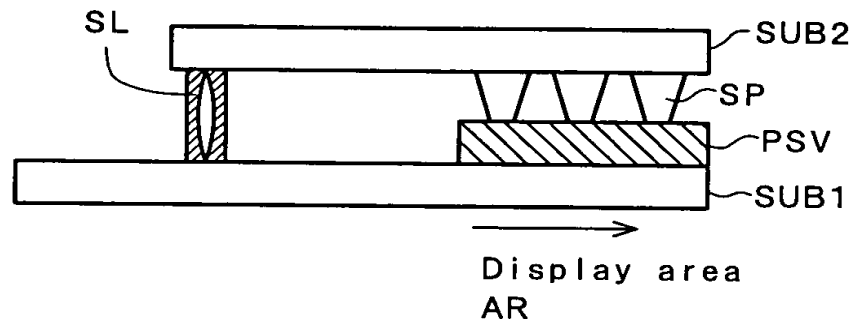


FIG. 29

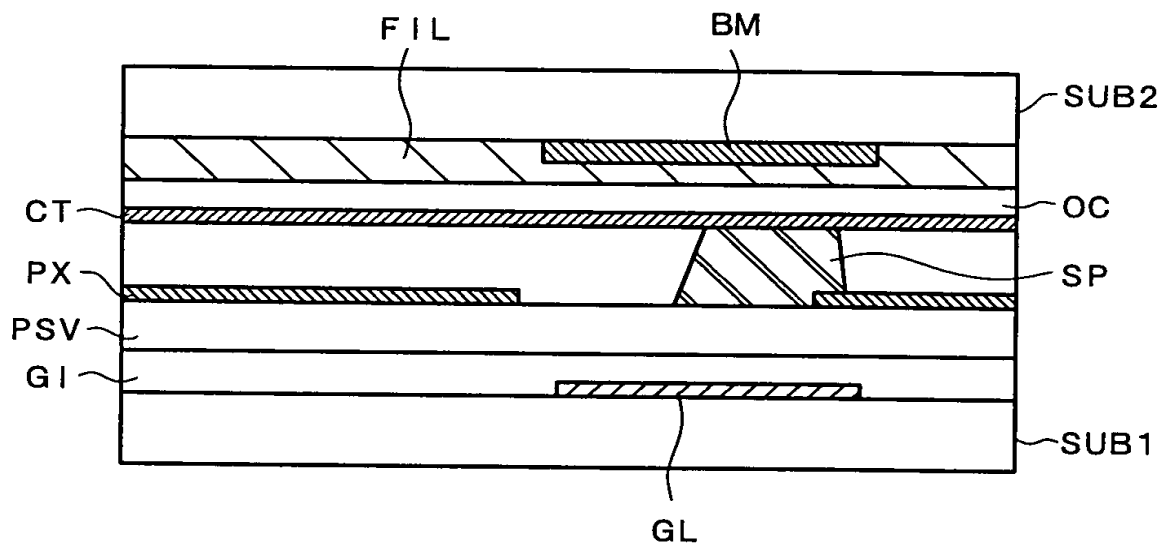


FIG. 30A

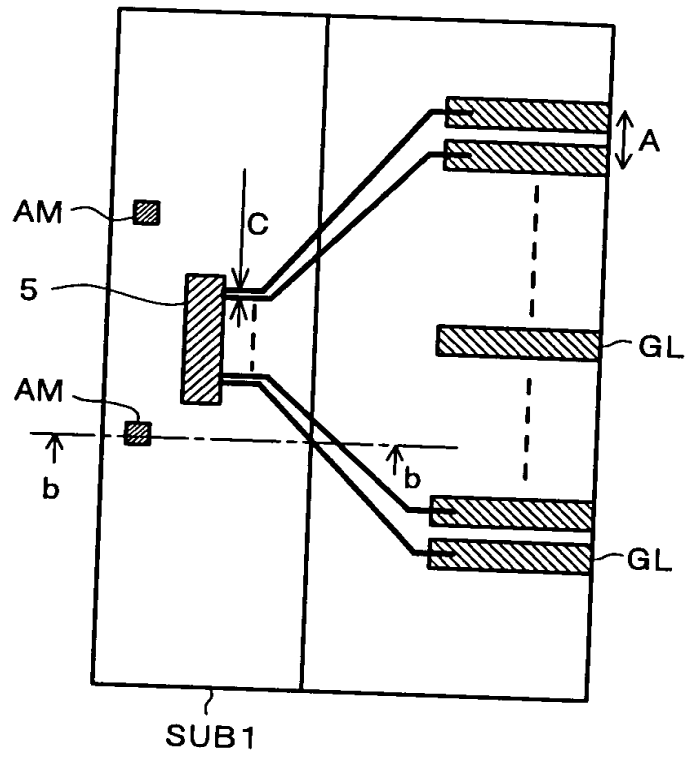


FIG. 30B

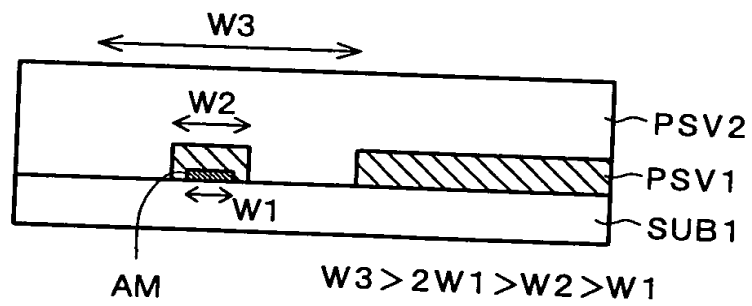


FIG. 31A

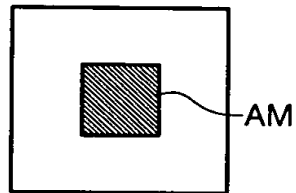


FIG. 31B

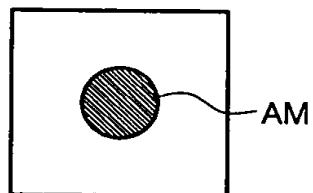


FIG. 31C

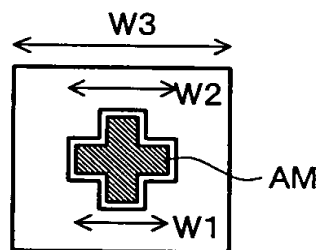


FIG. 32

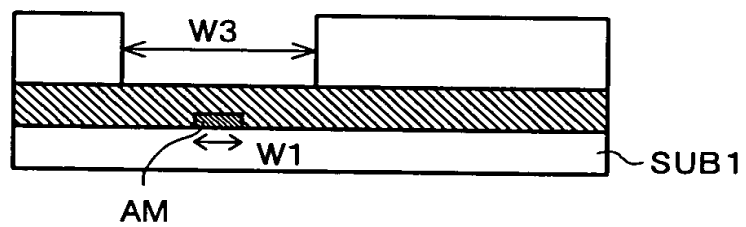


FIG. 33

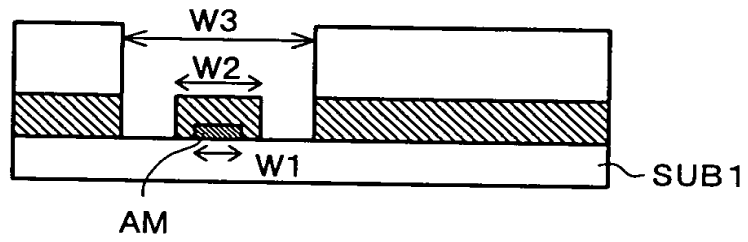


FIG. 34

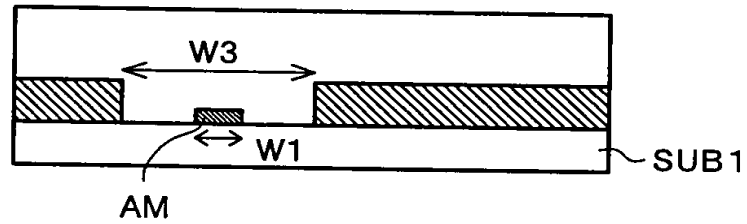


FIG. 35

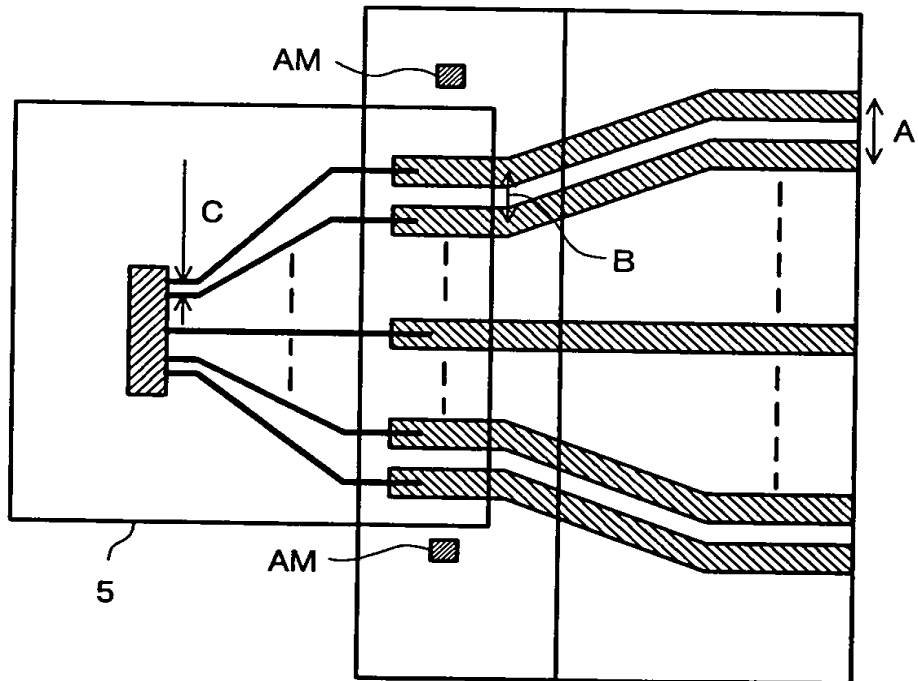


FIG. 36A

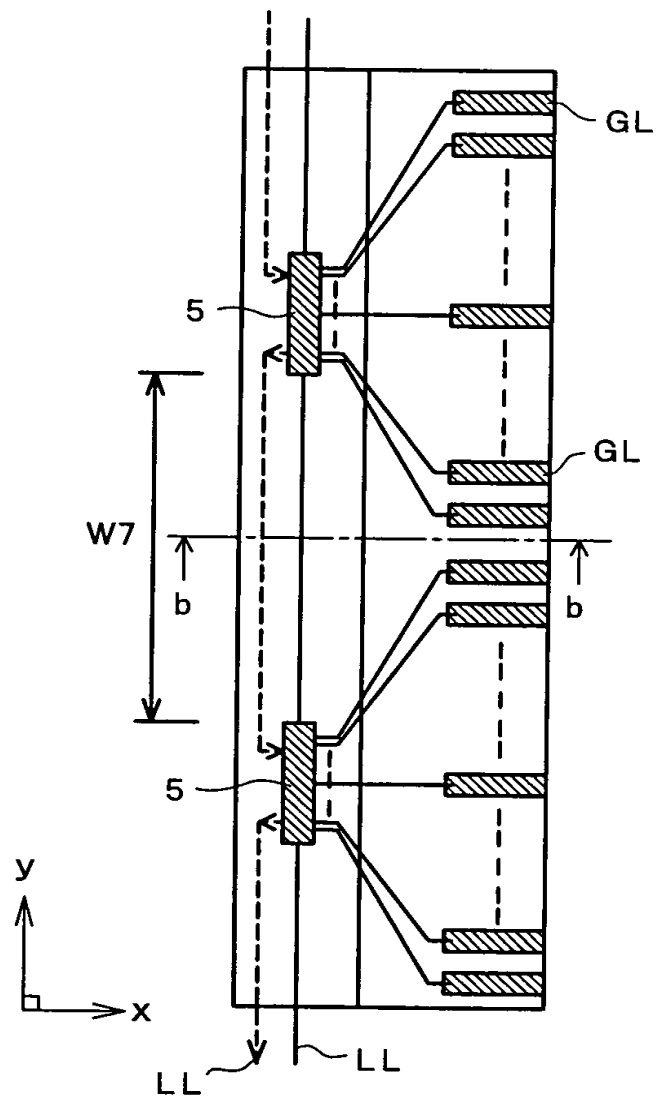


FIG. 36B

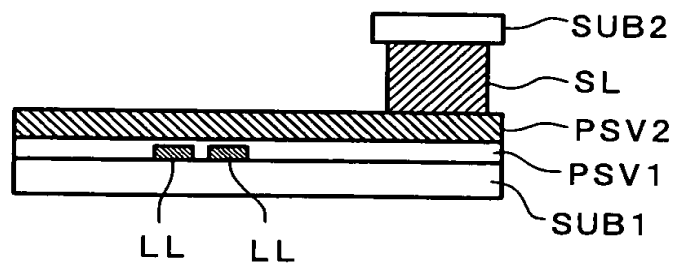


FIG. 37A

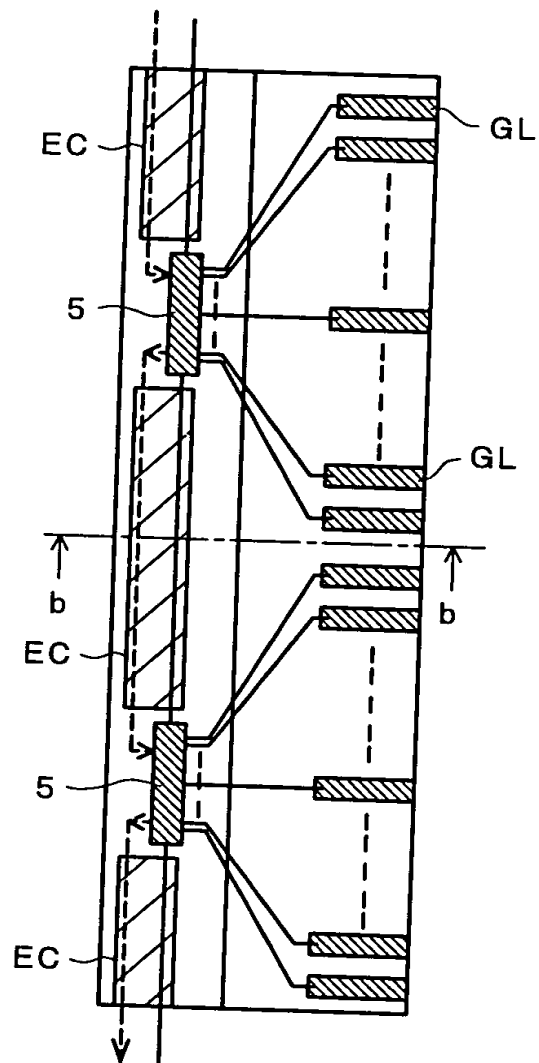


FIG. 37B

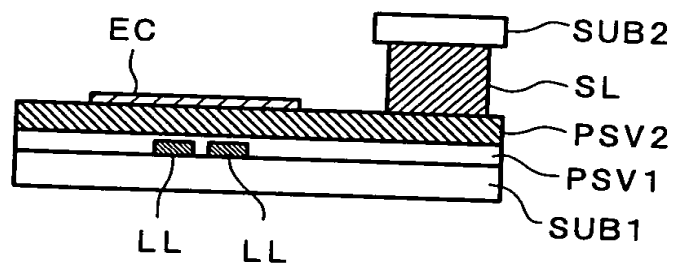


FIG. 38A

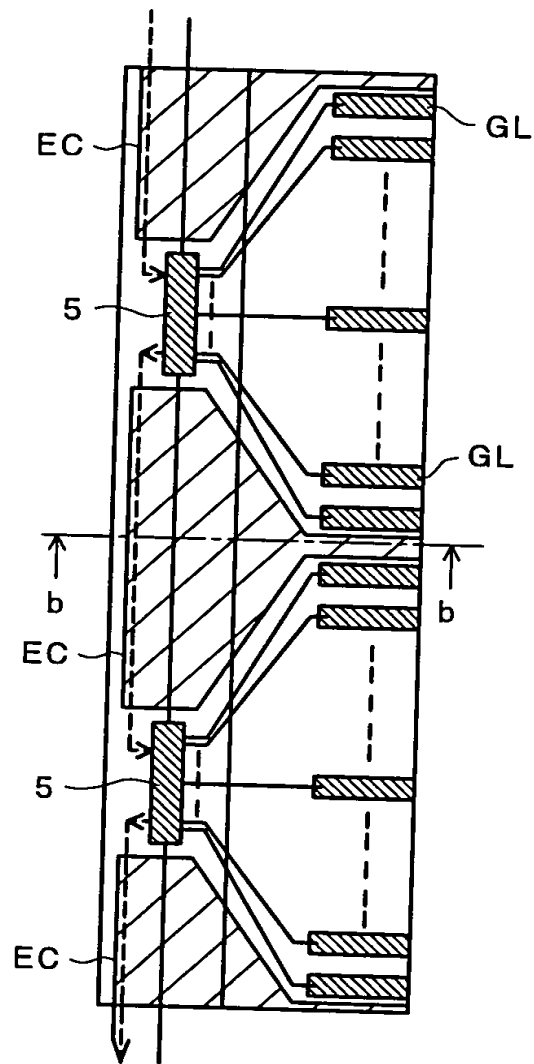


FIG. 38B

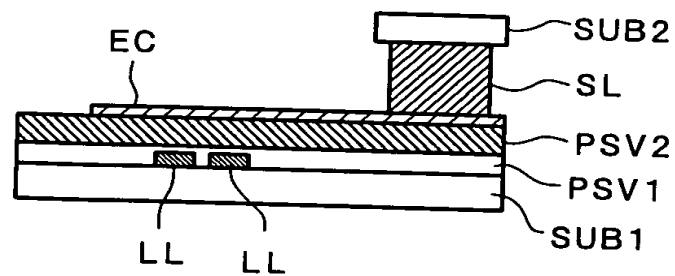


FIG. 39A

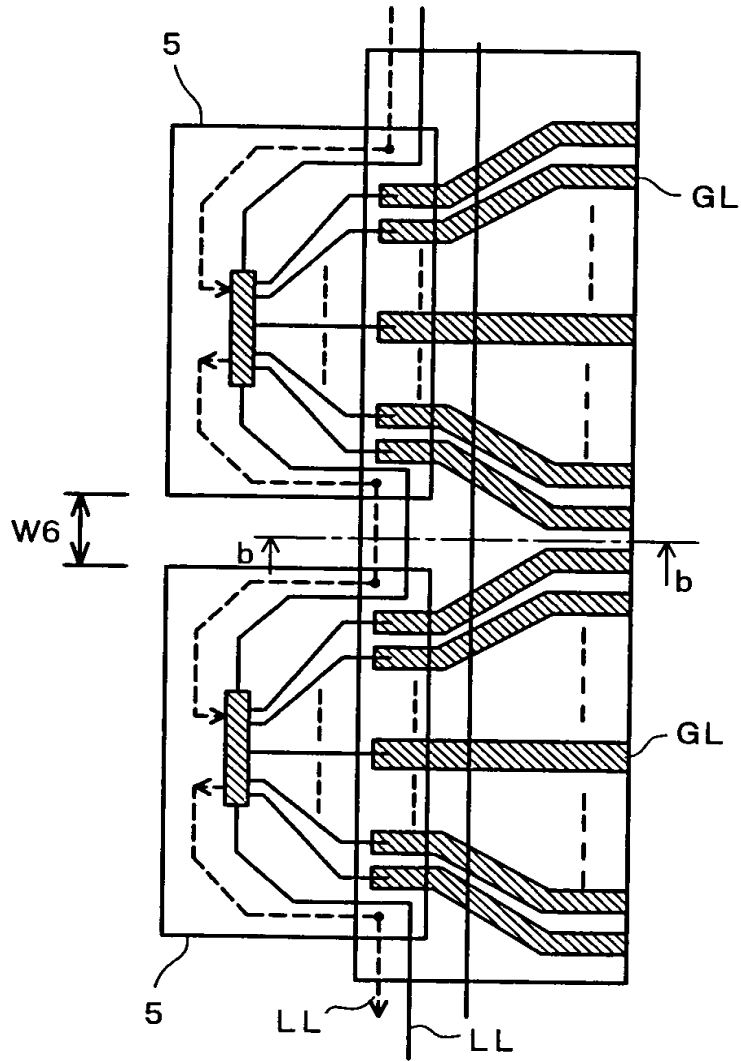


FIG. 39B

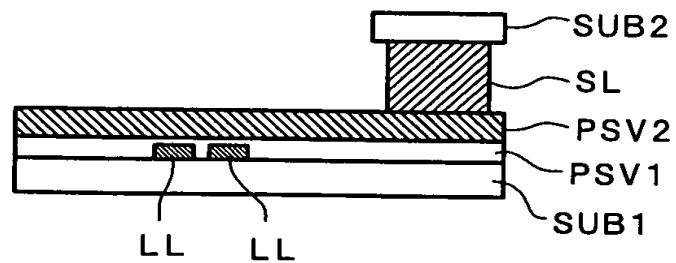


FIG. 40

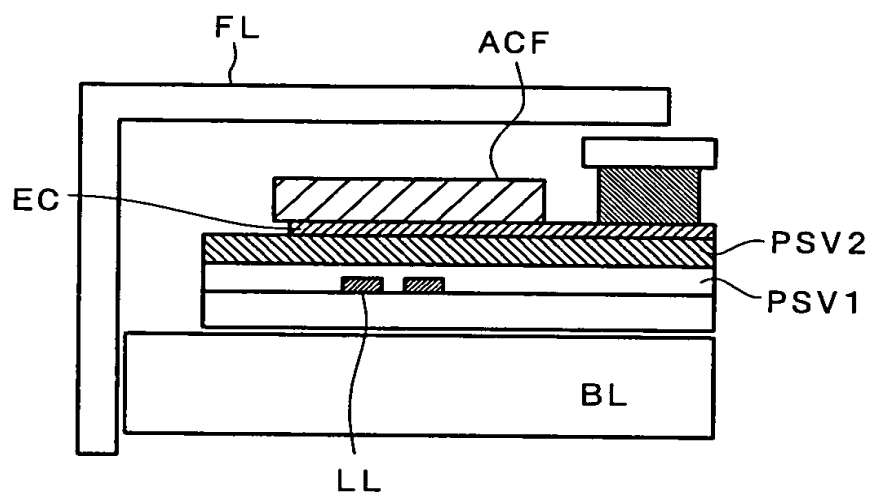


FIG. 41

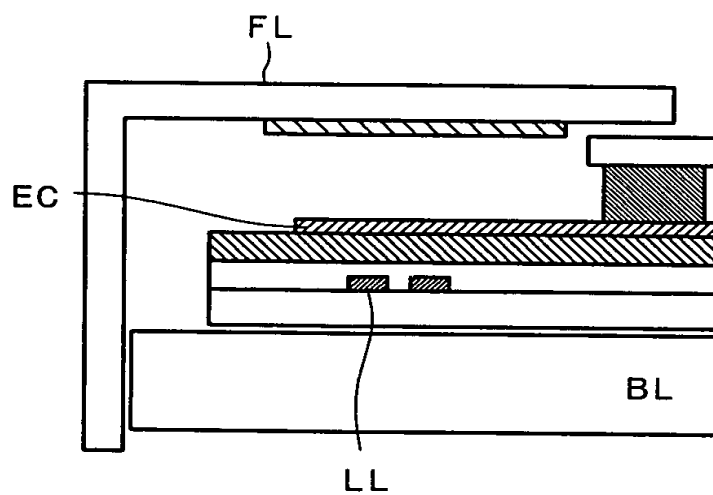


FIG. 42

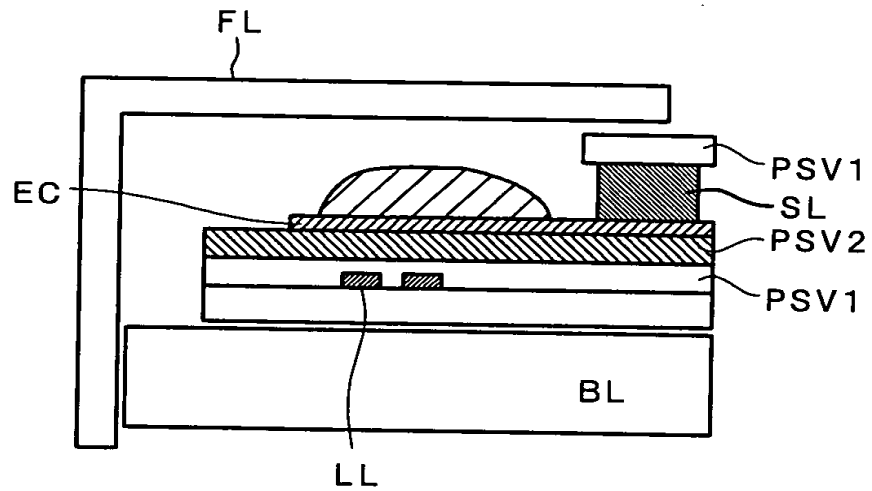


FIG. 43

